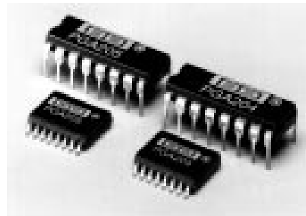
BURR - BROWN®



PGA204
PGA205

Programmable Gain
INSTRUMENTATION AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAIN:**
  PGA204: G=1, 10, 100, 1000V/V
  PGA205: G=1, 2, 4, 8V/V
- **LOW OFFSET VOLTAGE: 50µV max**
- **LOW OFFSET VOLTAGE DRIFT: 0.25µV/°C**
- **LOW INPUT BIAS CURRENT: 2nA max**
- **LOW QUIESCENT CURRENT: 5.2mA typ**
- **NO LOGIC SUPPLY REQUIRED**
- **16-PIN PLASTIC DIP, SOL-16 PACKAGES**

APPLICATIONS

- **DATA ACQUISITION SYSTEM**
- **GENERAL PURPOSE ANALOG BOARDS**
- **MEDICAL INSTRUMENTATION**

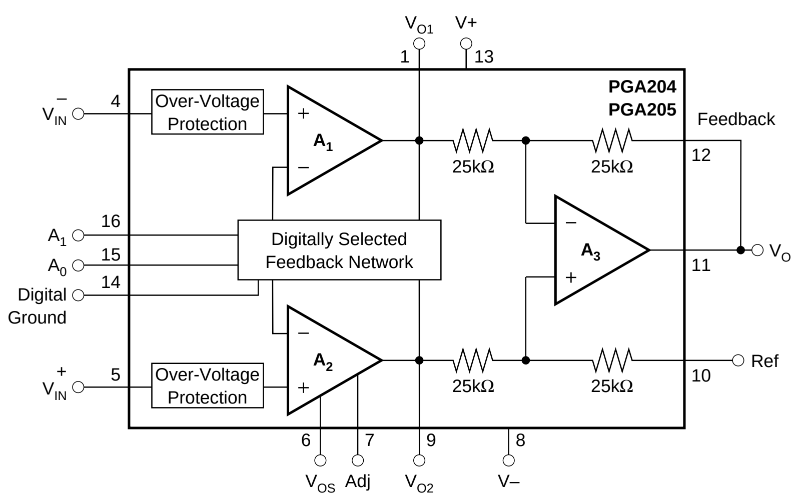
DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and low cost of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines, A_0 and A_1. Internal input protection can withstand up to ±40V on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G=1000). They operate with power supplies as low as ±4.5V, allowing use in battery operated systems. Quiescent current is 5mA.

The PGA204 and PGA205 are available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



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 PDS-1176A Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL PGA204 G=1, 10, 100, 1000V/V

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ unless otherwise noted.

		PGA204BP, BU			PGA204AP, AU			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
Offset Voltage, RTI	T_A=+25°C		±10+20/G	±50+100/G		±25+30/G	±125+500/G	μV
vs Temperature	T_A=T_{MIN} to T_{MAX}		±0.1+0.5/G	±0.25+5/G		±0.25+5/G	±1+10/G	μV/°C
vs Power Supply	V_S=±4.5V to ±18V		0.5+2/G	3+10/G		*	*	μV/V
Long-Term Stability			±0.2+0.5/G			*		μV/mo
Impedance, Differential			10^{10} ‖ 6			*		Ω ‖ pF
Common-Mode			10^{10} ‖ 6			*		Ω ‖ pF
Input Common-Mode Range	V_O=0V (see text)	±10.5	±12.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM}=±10V, ΔR_S=1kΩ							
	G=1	80	99		75	90		dB
	G=10	96	114		90	106		dB
	G=100	110	123		106	110		dB
	G=1000	115	123		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
Offset Current			±0.5	±2		*	*	nA
vs Temperature			±8			*		pA/°C
NOISE, Voltage, RTI(1): f=10Hz	G≥100, R_S=0Ω		16			*		nV/√Hz
f=100Hz	G≥100, R_S=0Ω		13			*		nV/√Hz
f=1kHz	G≥100, R_S=0Ω		13			*		nV/√Hz
f_B=0.1Hz to 10Hz	G≥100, R_S=0Ω		0.4			*		μVp-p
Noise Current								
f=10Hz			0.4			*		pA/√Hz
f=1kHz			0.2			*		pA/√Hz
f_B=0.1Hz to 10Hz			18			*		pAp-p
GAIN, Error	G=1		±0.005	±0.024		*	±0.05	%
	G=10		±0.01	±0.024		*	±0.05	%
	G=100		±0.01	±0.024		*	±0.05	%
	G=1000		±0.02	±0.05		*	±0.1	%
Gain vs Temperature	G=1 to 1000		±2.5	±10		*	*	ppm/°C
Nonlinearity	G=1		±0.0004	±0.001		*	±0.002	% of FSR
	G=10		±0.0004	±0.002		*	±0.004	% of FSR
	G=100		±0.0004	±0.002		*	±0.004	% of FSR
	G=1000		±0.0008	±0.01		*	±0.02	% of FSR
OUTPUT								
Voltage, Positive(2)	I_O=5mA, T_{MIN} to T_{MAX}	(V+)–1.5	(V+)–1.3		*	*		V
Negative(2)	I_O=–5mA, T_{MIN} to T_{MAX}	(V–)+1.5	(V–)+1.3		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+23/–17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1			*		MHz
	G=10		80			*		kHz
	G=100		10			*		kHz
	G=1000		1			*		kHz
Slew Rate	V_O=±10V, G=10	0.3	0.7		*	*		V/μs
Settling Time(3), 0.1%	G=1		22			*		μs
	G=10		23			*		μs
	G=100		100			*		μs
	G=1000		1000			*		μs
0.01%	G=1		23			*		μs
	G=10		28			*		μs
	G=100		140			*		μs
	G=1000		1300			*		μs
Overload Recovery	50% Overdrive		70			*		μs
DIGITAL LOGIC								
Digital Ground Voltage, V_{DG}		V–		(V+)–4	*		*	V
Digital Low Voltage		V–		V_{DG}+0.8V	*		*	V
Digital Input Current			1			*		μA
Digital High Voltage		V_{DG} +2		V+	*		*	V
POWER SUPPLY, Voltage		±4.5	±15	±18	*	*	*	V
Current	V_{IN}=0V		+5.2/–4.2	±6.5		*	±7.5	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.

SPECIFICATIONS

ELECTRICAL

PGA205 G=1, 2, 4, 8V/V

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ unless otherwise noted.

		PGA205BP, BU			PGA205AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI	T_A=+25°C		±10+20/G	±50+100/G		±25+30/G	±125+500/G	µV
vs Temperature	T_A=T_{MIN} to T_{MAX}		±0.1+0.5/G	±0.25+5/G		±0.25+5/G	±1+10/G	µV/°C
vs Power Supply	V_S=±4.5V to ±18V		0.5+2/G	3+10/G		*	*	µV/V
Long-Term Stability			±0.2+0.5/G			*		µV/mo
Impedance, Differential			10^{10}‖6			*		Ω‖pF
Common-Mode			10^{10}‖6			*		Ω‖pF
Input Common-Mode Range	V_O=0V (see text)	±10.5	±12.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM}=±10V, ΔR_S=1kΩ							
	G=1	80	94		75	88		dB
	G=2	85	100		80	94		dB
	G=4	90	106		85	100		dB
	G=8	95	112		89	106		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
Offset Current			±0.5	±2		*	*	nA
vs Temperature			±8			*		pA/°C
Noise Voltage, RTI(1): f=10Hz	G=8, R_S=0Ω		19			*		nV/√Hz
f=100Hz	G=8, R_S=0Ω		15			*		nV/√Hz
f=1kHz	G=8, R_S=0Ω		15			*		nV/√Hz
f_B=0.1Hz to 10Hz	G=8, R_S=0Ω		0.5			*		µVp-p
Noise Current								
f=10Hz			0.4			*		pA/√Hz
f=1kHz			0.2			*		pA/√Hz
f_B=0.1Hz to 10Hz			18			*		pAp-p
GAIN, Error	G=1		±0.005	±0.024		*	±0.05	%
	G=2		±0.01	±0.024		*	±0.05	%
	G=4		±0.01	±0.024		*	±0.05	%
	G=8		±0.01	±0.024		*	±0.05	%
Gain vs Temperature	G=1 to 8		±2.5	±10		*	*	ppm/°C
Nonlinearity	G=1		±0.00024	±0.001		*	±0.002	% of FSR
	G=2		±0.00024	±0.002		*	±0.004	% of FSR
	G=4		±0.00024	±0.002		*	±0.004	% of FSR
	G=8		±0.00024	±0.002		*	±0.004	% of FSR
OUTPUT								
Voltage, Positive(2)	I_O=5mA, T_{MIN} to T_{MAX}	(V+)–1.5	(V+)–1.3		*	*		V
Negative(2)	I_O=–5mA, T_{MIN} to T_{MAX}	(V–)+1.5	(V–)+1.3		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+23/–17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1			*		MHz
	G=2		400			*		kHz
	G=4		200			*		kHz
	G=8		100			*		kHz
Slew Rate	V_O=±10V, G=8	0.3	0.7		*	*		V/µs
Settling Time(3), 0.1%	G=1		22			*		µs
	G=2		22			*		µs
	G=4		23			*		µs
	G=8		23			*		µs
0.01%	G=1		23			*		µs
	G=2		23			*		µs
	G=4		25			*		µs
	G=8		28			*		µs
Overload Recovery	50% overdrive		70			*		µs
DIGITAL LOGIC INPUTS								
Digital Ground Voltage, V_{DG}		V–		(V+)–4	*		*	V
Digital Low Voltage		V–		V_{DG}+0.8V	*		*	V
Digital Low Current			1			*		µA
Digital High Voltage		V_{DG}+2		V+	*		*	V
POWER SUPPLY, Voltage		±4.5	±15	±18	*	*	*	V
Current	V_{IN}=0V		+5.2/–4.2	±6.5		*	±7.5	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
θ_{JA}			80			*		°C/W

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for ±10V min on ±11.4V power supplies. (3) Includes time to switch to a new gain.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA204AP	16-Pin Plastic DIP	180
PGA204BP	16-Pin Plastic DIP	180
PGA204AU	SOL-16 Surface Mount	211
PGA204BU	SOL-16 Surface Mount	211
PGA205AP	16-Pin Plaseic DIP	180
PGA205BP	16-Pin Plastic DIP	180
PGA205AU	SOL-16 Surface Mount	211
PGA205BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

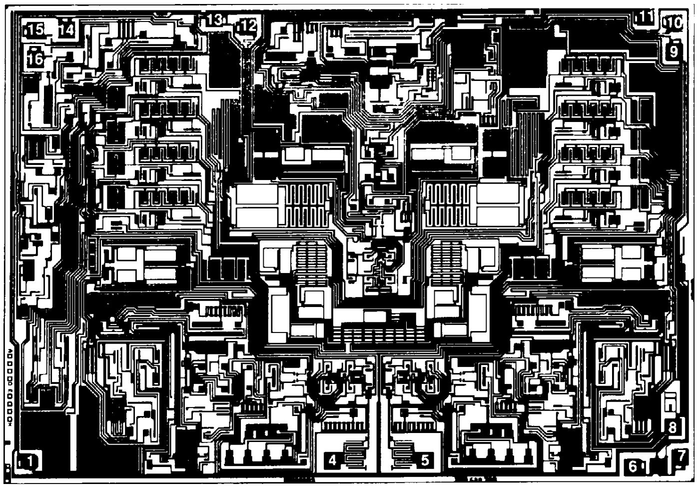
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA204AP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	–40 to +85°C
PGA204BP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	–40 to +85°C
PGA204AU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA204BU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA205AP	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40 to +85°C
PGA205BP	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40 to +85°C
PGA205AU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40 to +85°C
PGA205BU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40 to +85°C

DICE INFORMATION



PGA204/205 DIE TOPOGRAPHY

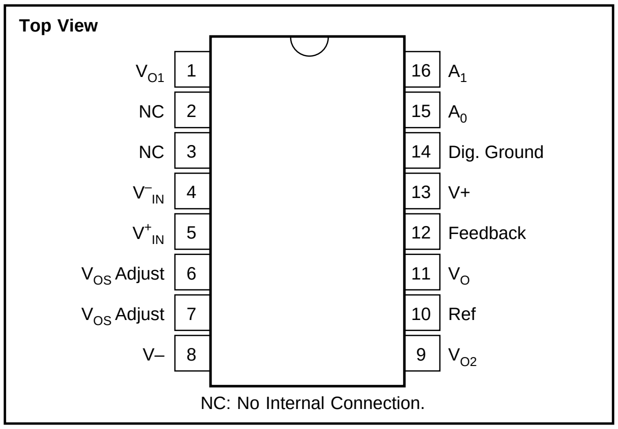
PAD	FUNCTION	PAD	FUNCTION
1	V_{O1}	9	V_{O2}
2	—	10	Ref
3	—	11	V_O
4	V^-_{IN}	12	Feedback
5	V^+_{IN}	13	V+
6	V_{OS} Adj	14	Dig. Ground
7	V_{OS} Adj	15	A_0
8	V–	16	A_1

Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	186 x 130 ±5	4.72 x 3.30 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

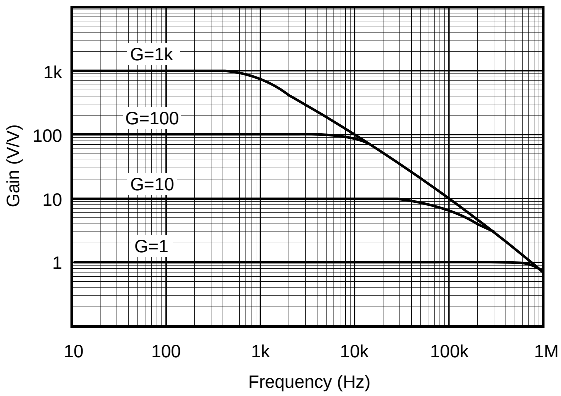
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

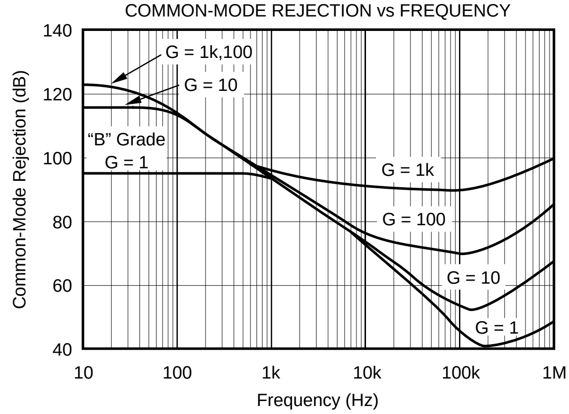
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, and $V_S = ±15V$, unless otherwise noted.

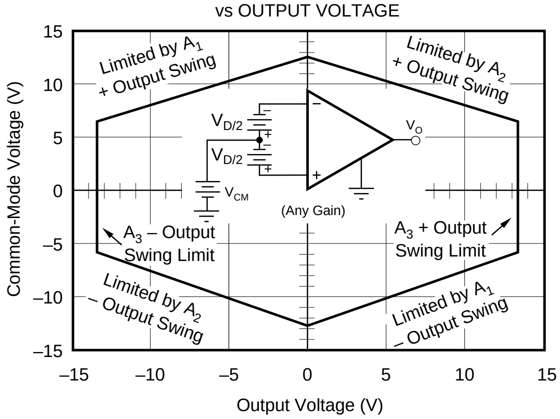
GAIN vs FREQUENCY



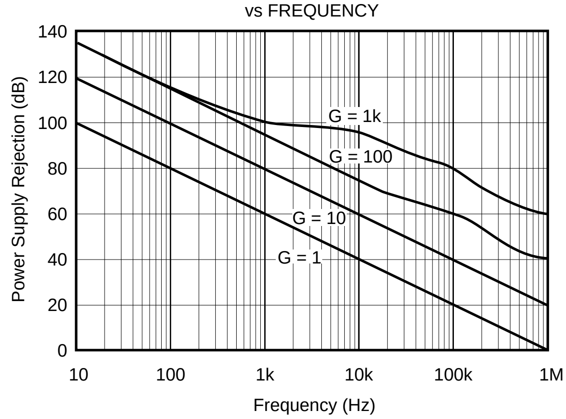
COMMON-MODE REJECTION vs FREQUENCY



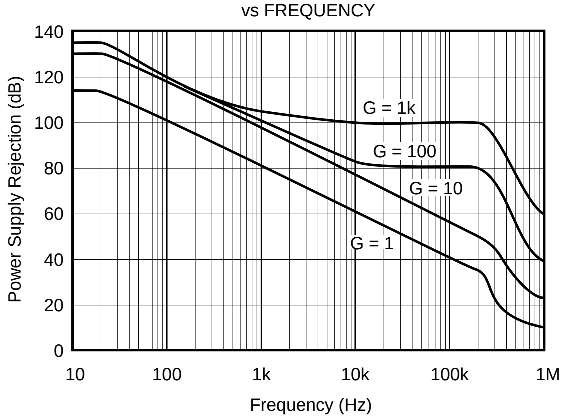
INPUT COMMON-MODE VOLTAGE RANGE
vs OUTPUT VOLTAGE



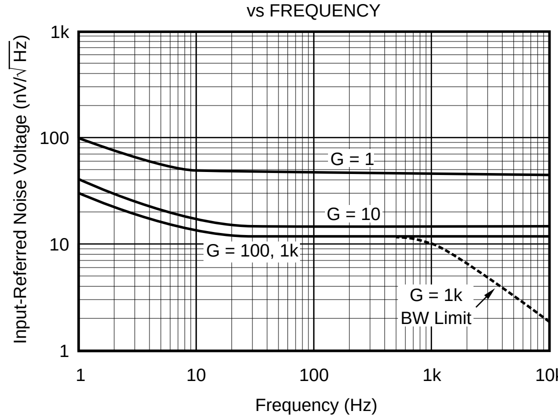
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



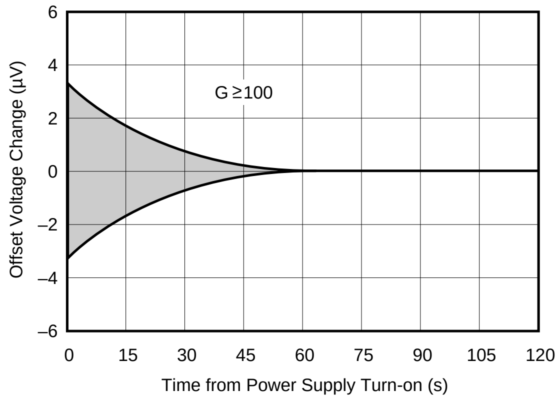
INPUT- REFERRED NOISE VOLTAGE
vs FREQUENCY



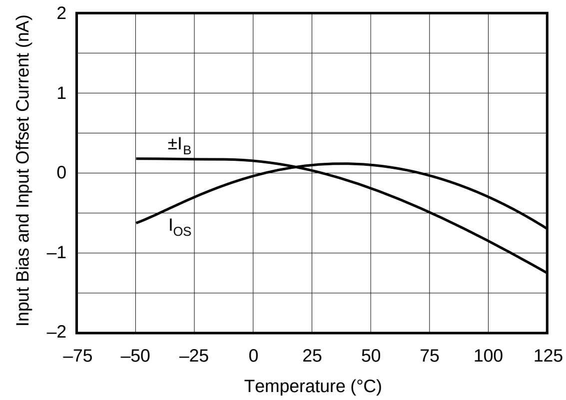
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

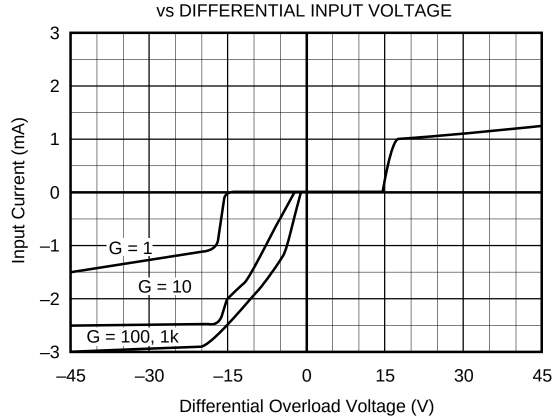
INPUT-REFERRED
OFFSET VOLTAGE WARM-UP vs TIME



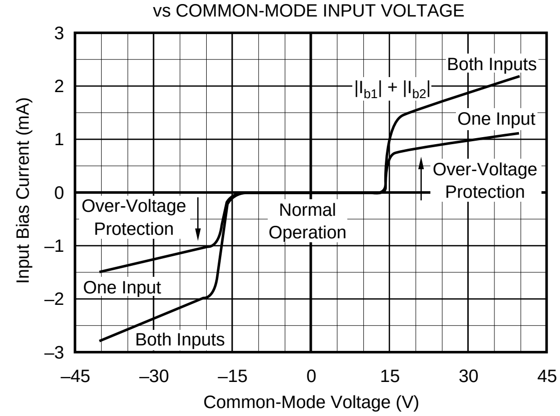
INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



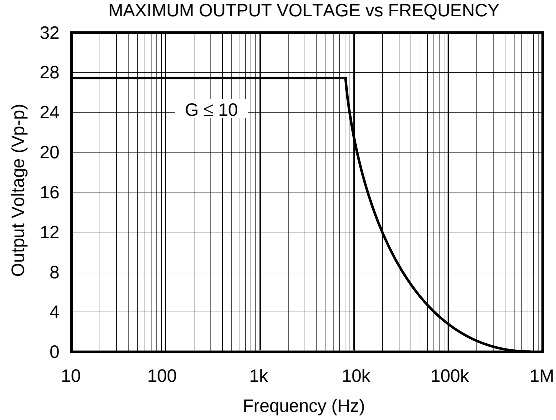
INPUT BIAS CURRENT
vs DIFFERENTIAL INPUT VOLTAGE



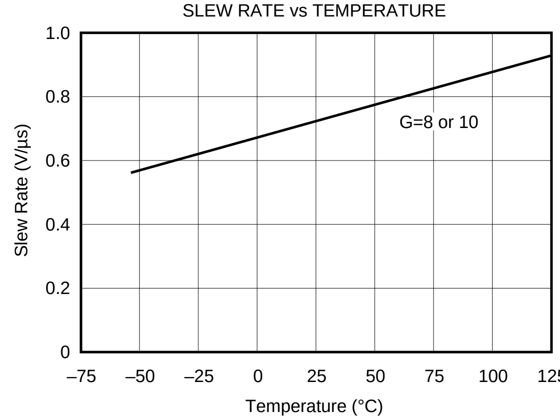
INPUT BIAS CURRENT
vs COMMON-MODE INPUT VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

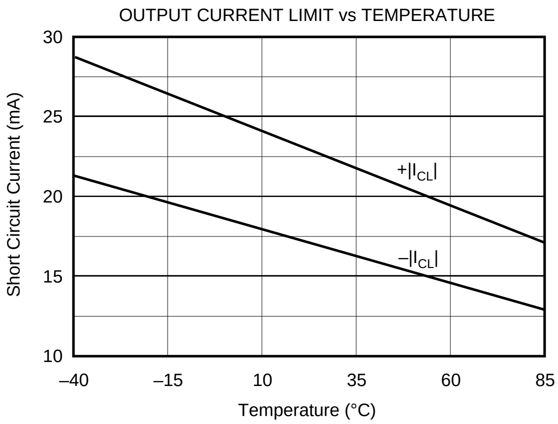


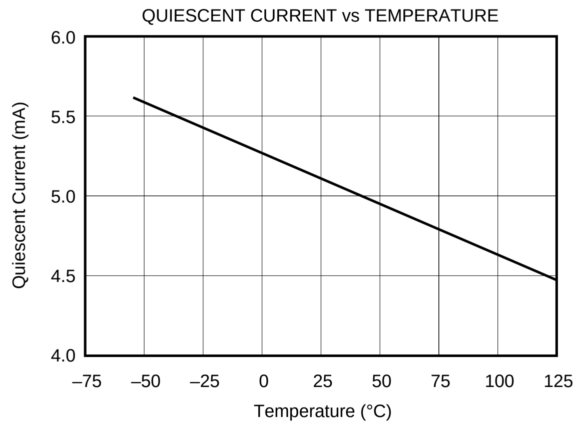
SLEW RATE vs TEMPERATURE

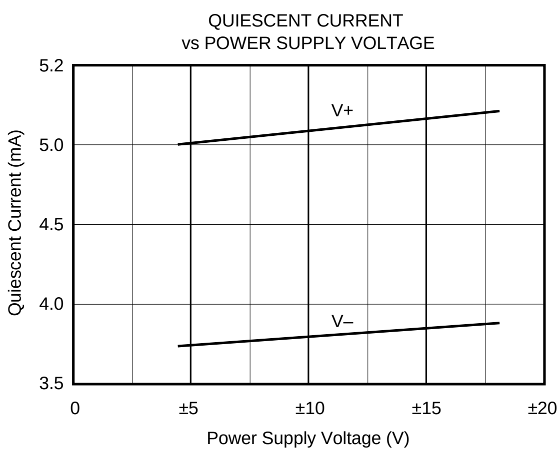


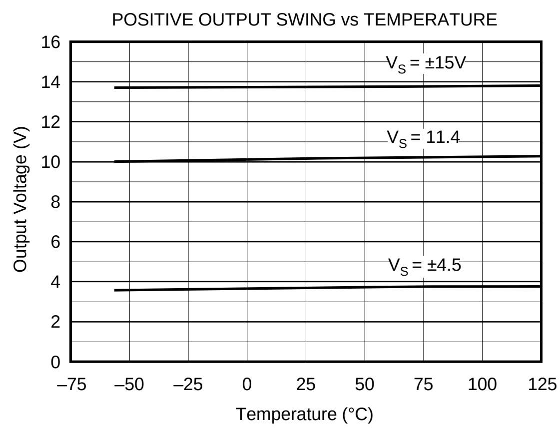
TYPICAL PERFORMANCE CURVES (CONT)

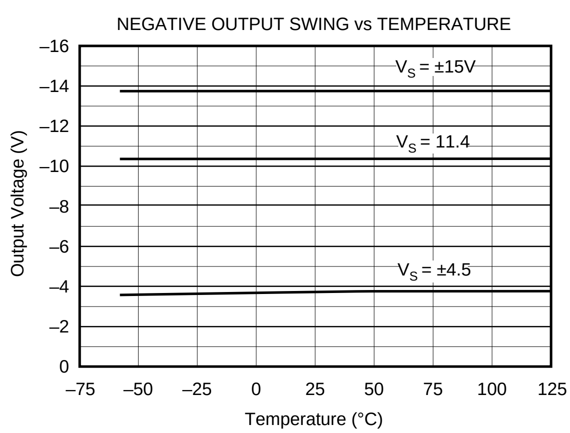
At T_A = +25°C, and V_S = ±15V, unless otherwise noted.







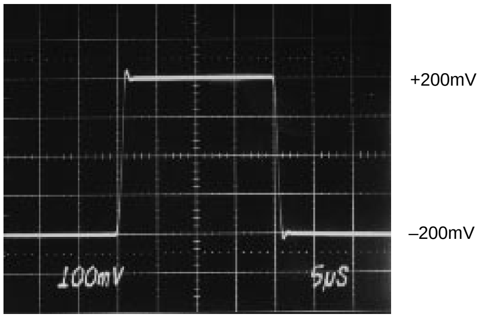




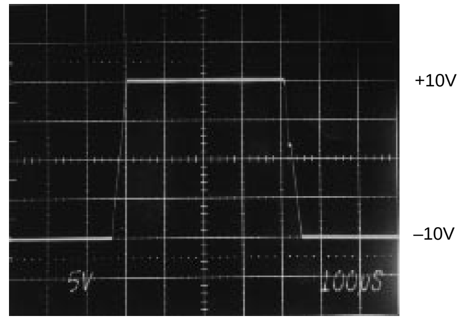
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

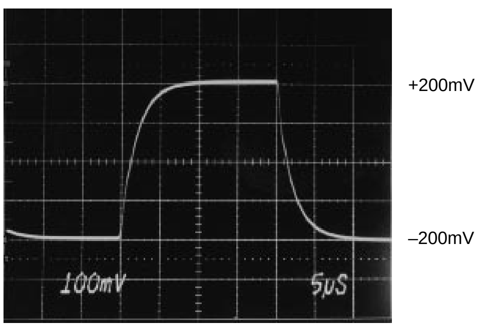
SMALL-SIGNAL RESPONSE, G = 1



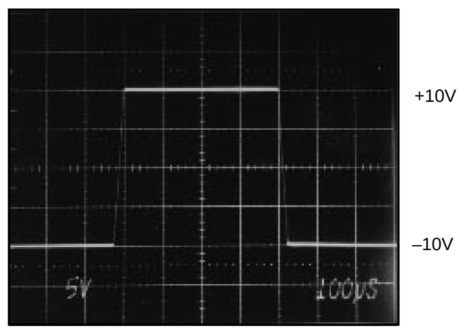
LARGE-SIGNAL RESPONSE, G = 1



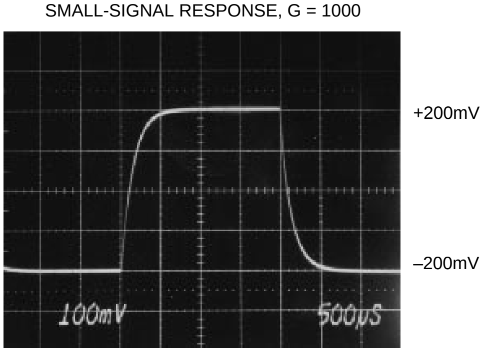
SMALL-SIGNAL RESPONSE, G = 10



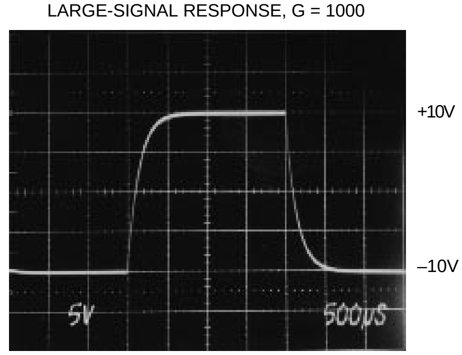
LARGE-SIGNAL RESPONSE, G = 10



SMALL-SIGNAL RESPONSE, G = 1000



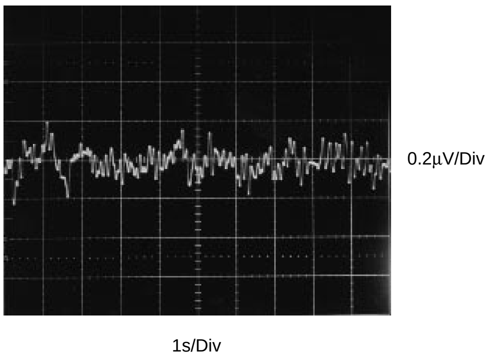
LARGE-SIGNAL RESPONSE, G = 1000



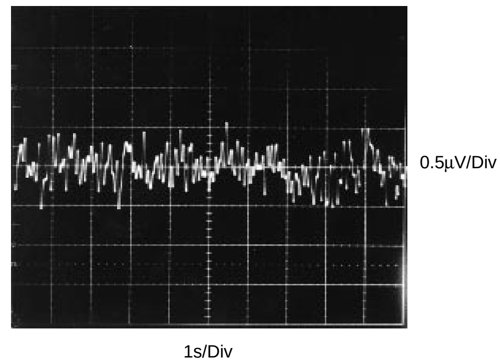
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, and $V_S = ±15V$, unless otherwise noted.

INPUT-REFERRED NOISE,
0.1 TO 10Hz, G = 1000



NOISE, 0.1 TO 10Hz, G = 1



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA204/205. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

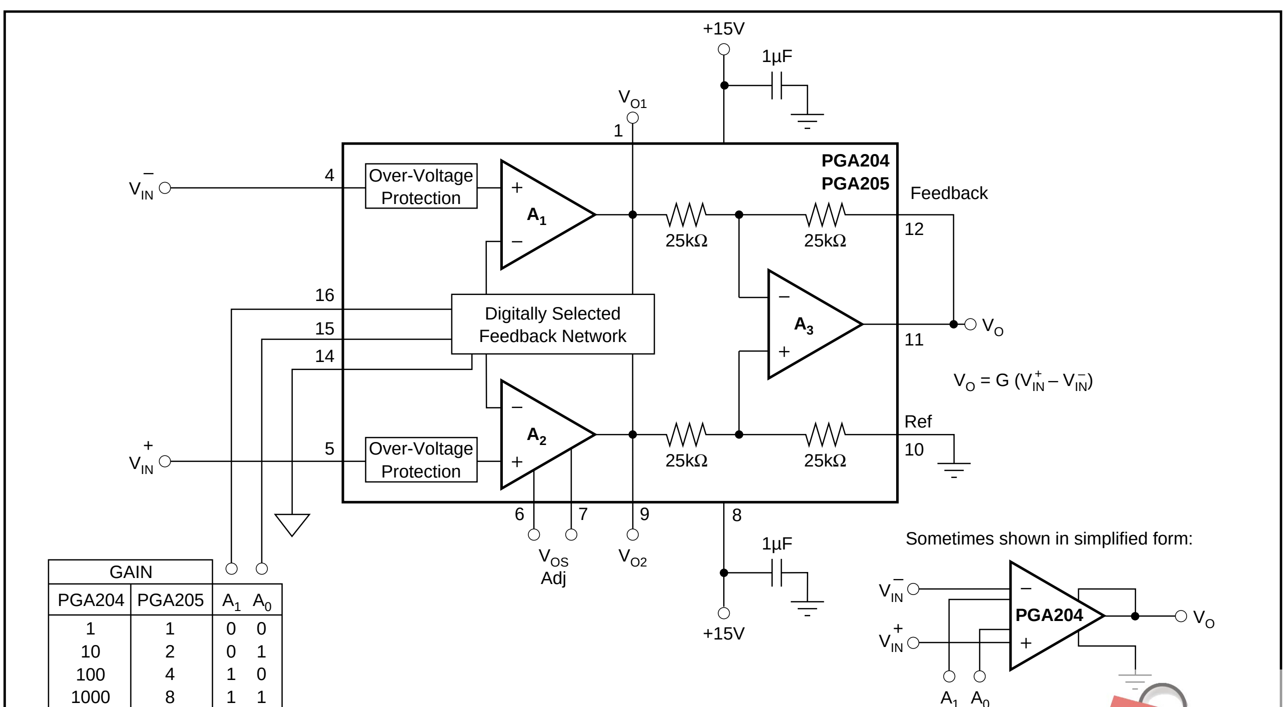
The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The PGA204/205 has an output feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. The output Feedback connection can be used to sense the output voltage directly at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential from the V– power supply to 4V less than V+. Digital ground is normally connected to ground. The digital inputs interface directly CMOS and TTL logic components.

Approximately 1µA flows out of the digital input pins when a logic "0" is applied. Logic input current is nearly zero with a logic "1" input. A constant current of approximately



GAIN			
PGA204	PGA205	A_1	A_0
1	1	0	0
10	2	0	1
100	4	1	0
1000	8	1	1

FIGURE 1. Basic Connections.

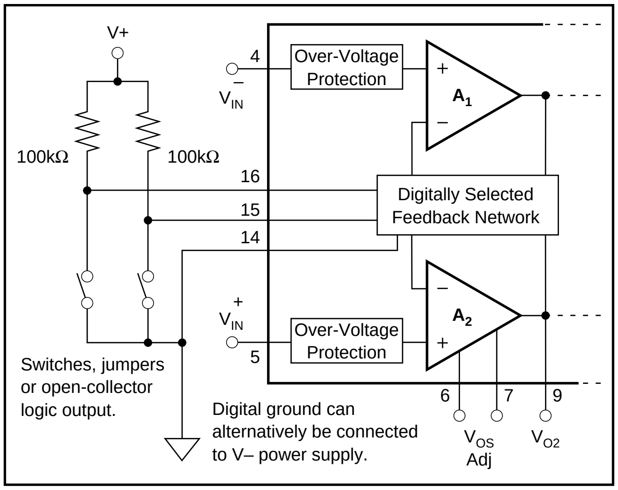


FIGURE 2. Switch or Jumper-Selected Digital Inputs.

1.3mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1, are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1µs. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control data from a high speed data bus (see Figure 7). Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry.

Some applications select gain of the PGA204/205 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch, jumper or open-collector logic is open or off. Fixed-gain applications can connect the logic inputs directly to V+ or V– (or other valid logic level); no resistor is required.

OFFSET VOLTAGE

Voltage offset of the PGA204/205 consists of two components—input stage offset and output stage offset. Both components are specified in the specification table in equation form:

$$V_{OS} = V_{OSI} + V_{OSO} / G \quad (1)$$

where:

V_{OS} total is the combined offset, referred to the input.

V_{OSI} is the offset voltage of the input stage, A_1 and A_2.

V_{OSO} is the offset voltage of the output difference amplifier, A_3.

V_{OSI} and V_{OSO} do not change with gain. The composite offset voltage V_{OS} changes with gain because of the gain term in equation 1. Input stage offset dominates in high gain (G≥100); both sources of offset may contribute at low gain (G=1 to 10).

OFFSET TRIMMING

Both the input and output stages are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment.

Figure 3 shows an optional input offset voltage trim circuit. This circuit should be used to adjust only the input stage offset voltage of the PGA204/205. Do this by programming

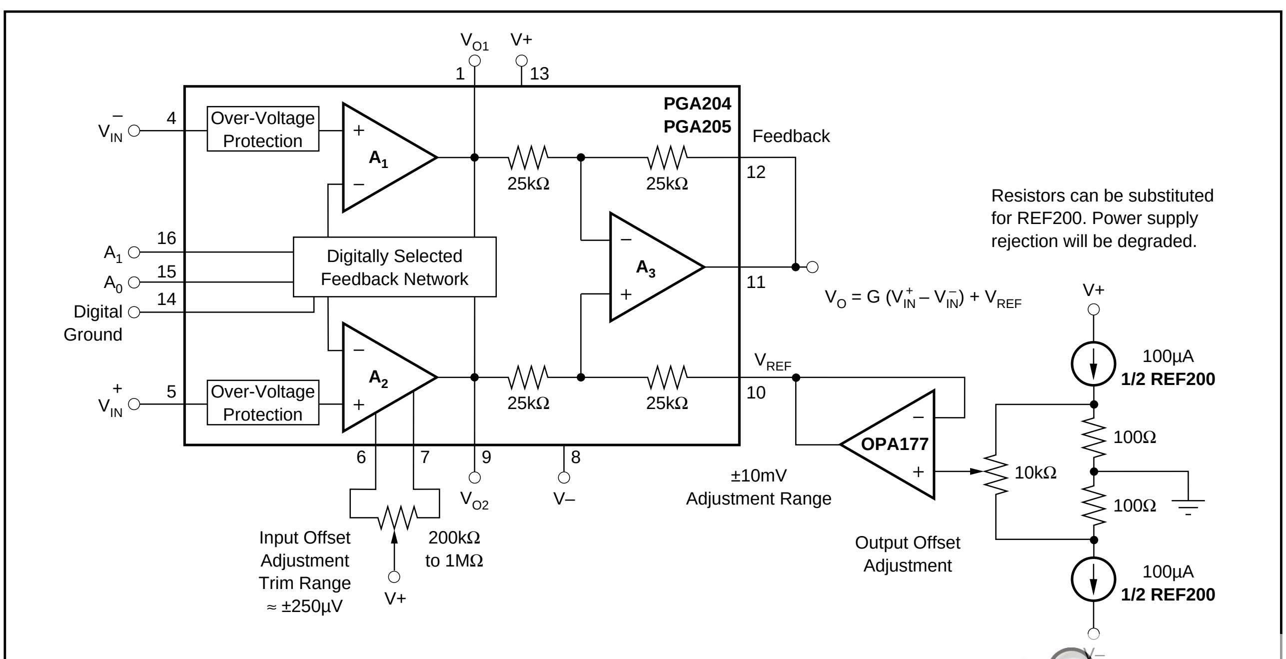


FIGURE 3. Optional Offset Voltage Trim Circuit.

it to its highest gain and trimming the output voltage to zero with the inputs grounded. Drift performance usually improves slightly when the input offset is nulled with this procedure.

Do not use the input offset adjustment to trim system offset or offset produced by a sensor. Nulling offset that is not produced by the input amplifiers will increase temperature drift by approximately 3.3µV/°C per 1mV of offset adjustment.

Many applications that need input stage offset adjustment do not need output stage offset adjustment. Figure 3 also shows a circuit for adjusting output offset voltage. First, adjust the input offset voltage as discussed above. Then program the device for G=1 and adjust the output to zero. Because of the interaction of these two adjustments at G=8, the PGA205 may require iterative adjustment.

The output offset adjustment can be used to trim sensor or system offsets without affecting drift. The voltage applied to the Ref terminal is summed with the output signal. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

NOISE PERFORMANCE

The PGA204/205 provides very low noise in most applications. Low frequency noise is approximately 0.4µVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the PGA204/205 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the PGA204/205 is to operate properly. Figure 4 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the PGA204/205 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 4). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 4). These applications do not require additional resistor(s) for proper operation.

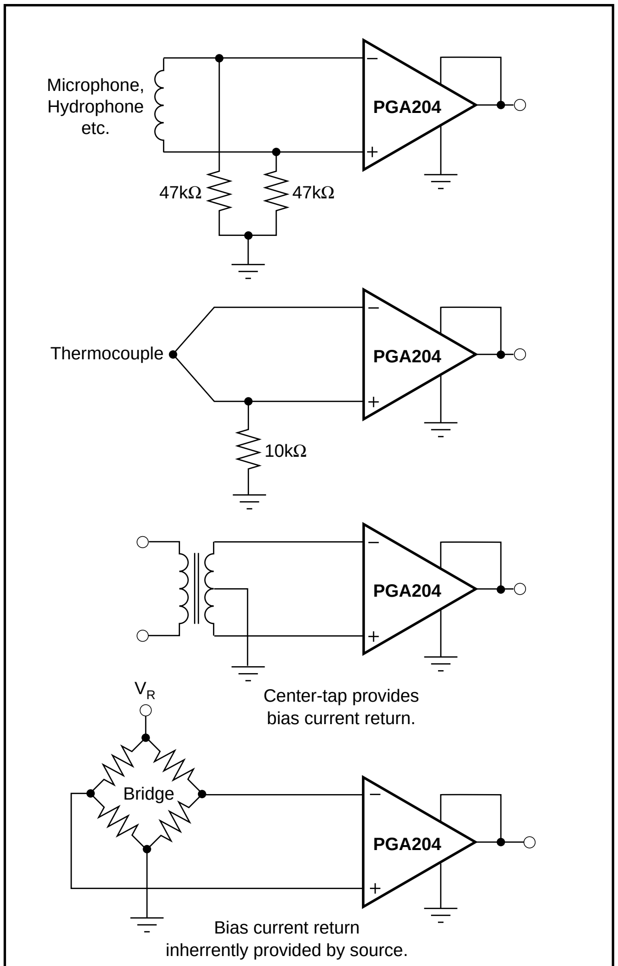


FIGURE 4. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the PGA204/205 is approximately ±12.7V (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage".

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 5 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the PGA204/205 (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the PGA204/205 to increase the voltage swing.

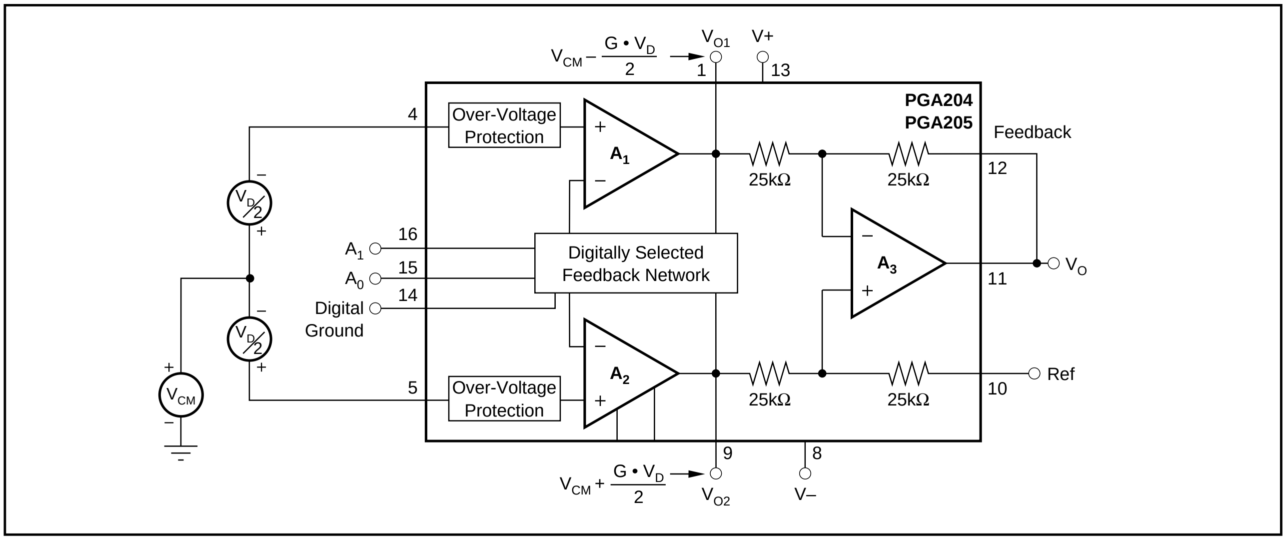
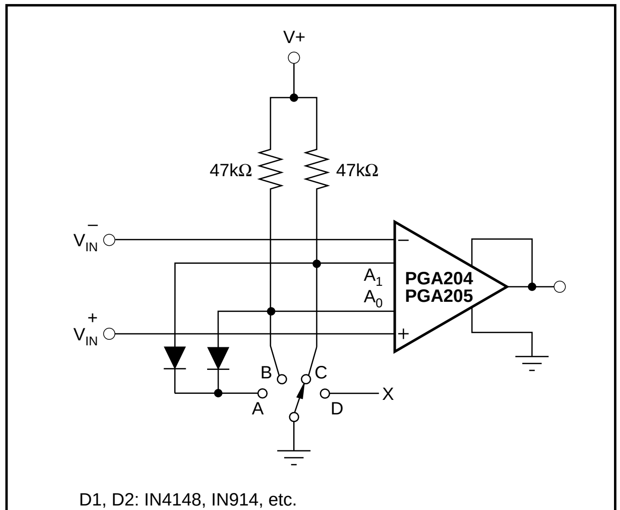


FIGURE 5. Voltage Swing of A_1 and A_2.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA204/205 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the PGA204/205 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.



SWITCH POSITION	GAIN	
	PGA204	PGA205
A	1	1
B	10	2
C	100	4
D	1000	8

FIGURE 6. Switch-Selected PGIA.

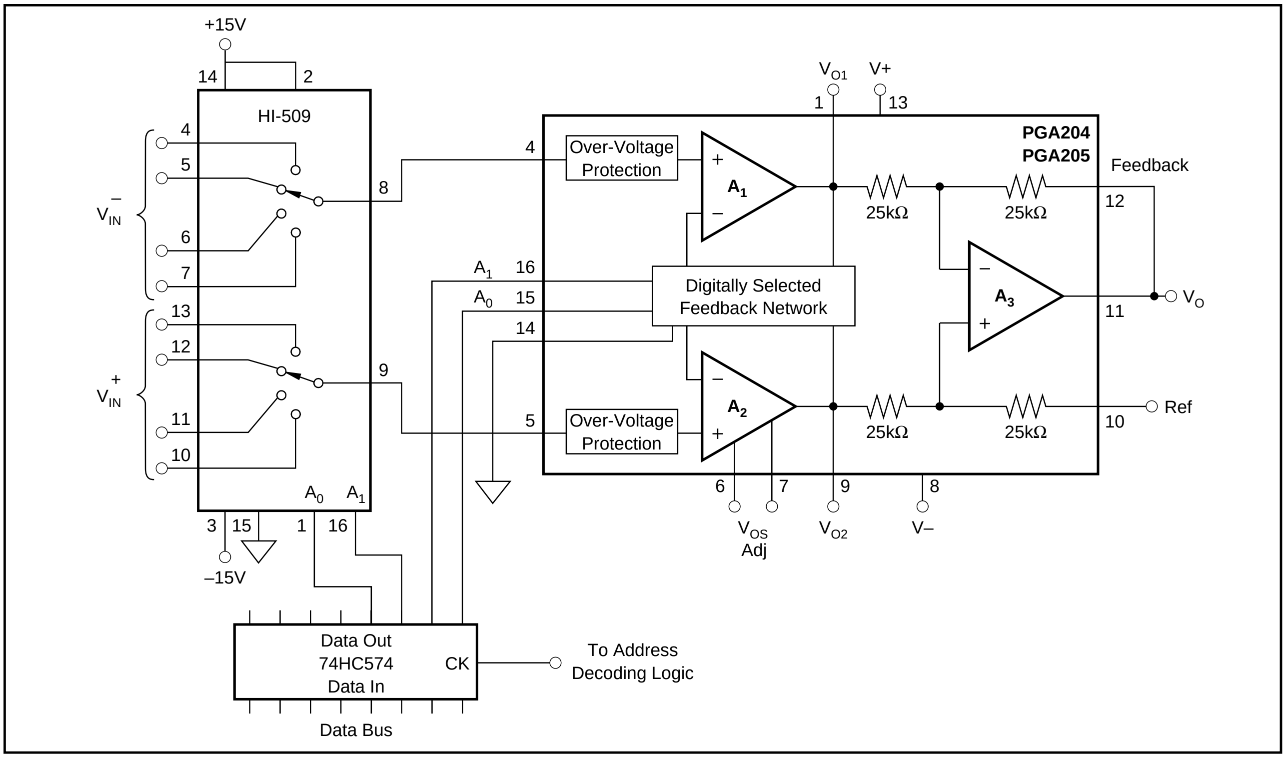


FIGURE 7. Multiplexed-Input Programmable Gain IA.

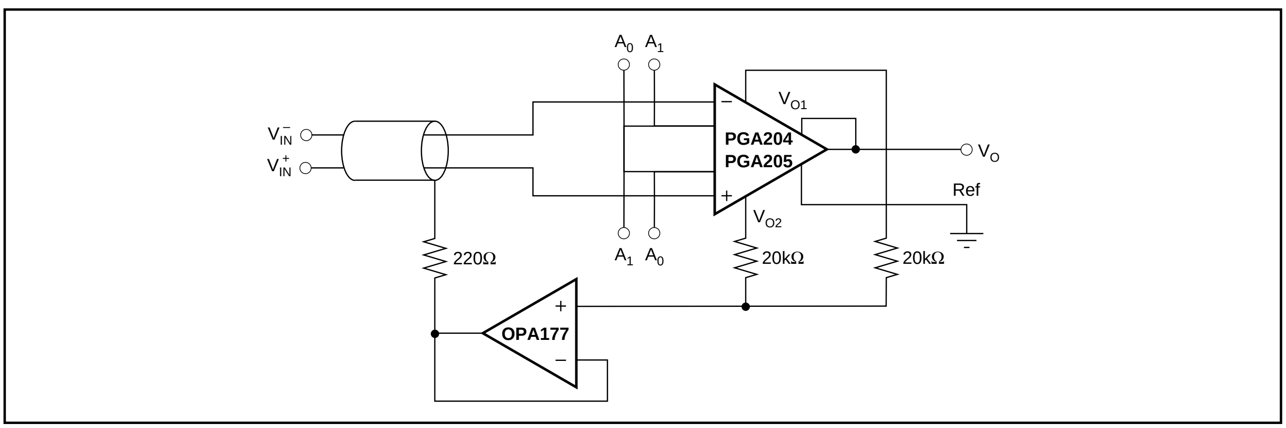
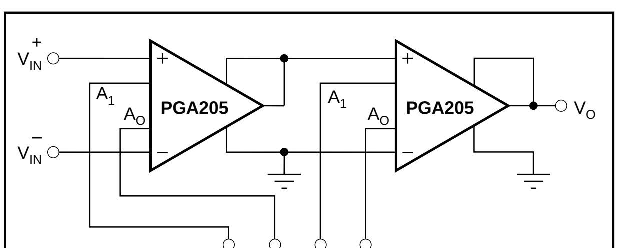


FIGURE 8. Shield Drive Circuit.



GAIN	A_3	A_2	A_1	A_0
1	0	0	0	0
2	0	1	0	0
4	1	0	0	0
8	1	1	0	0
16	1	1	0	1
32	1	1	1	0
64	1	1	1	1

FIGURE 9. Binary Gain Steps, G=1 to G=64.

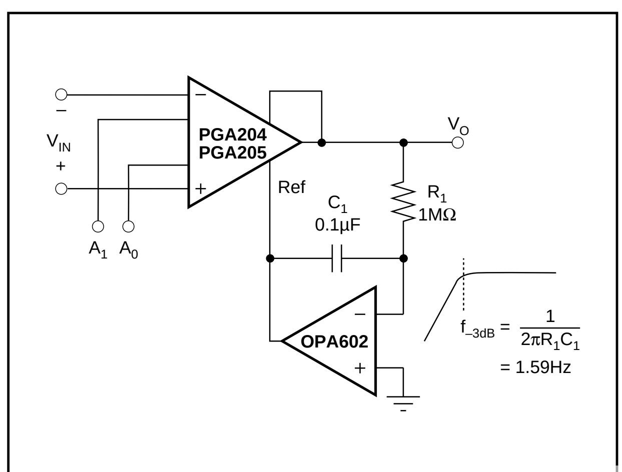


FIGURE 10. AC-Coupled PGIA.