NVD5C648NL

[MOSFET](http://www.onsemi.com) – Power, Single N-Channel

60 V, 4.1 mΩ, 89 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	4.1 mΩ @ 10 V	89 A
	5.7 mΩ @ 4.5 V	

N−CHANNEL MOSFET

DPAK
CASE 369C
STYLE 2

**MARKING DIAGRAM
& PIN ASSIGNMENT**

A	= Assembly Location
Y	= Year
WW	= Work Week
5C648L	= Device Code
G	= Pb−Free Package

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{θJC}$ (Notes 1 & 3)	Steady State	T_C = 25°C	I_D	89	A
		T_C = 100°C		63	
Power Dissipation $R_{θJC}$ (Note 1)		T_C = 25°C	P_D	72	W
		T_C = 100°C		36	
Continuous Drain Current $R_{θJA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	I_D	18	A
		T_A = 100°C		13	
Power Dissipation $R_{θJA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.5	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	510	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	85	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 7.0 A)			E_{AS}	223	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

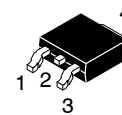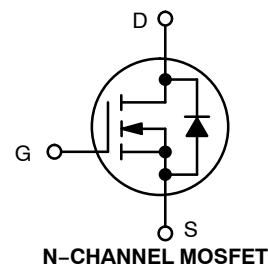| Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{θJC}$	2.07	°C/W
Junction−to−Ambient – Steady State (Note 2)	$R_{θJA}$	48.1	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.
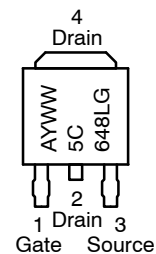
ORDERING INFORMATION

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				24		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 45 A			3.4	4.1	mΩ
		V_{GS} = 4.5 V, I_D = 45 A			4.6	5.7	
Forward Transconductance	g_{FS}	V_{DS} = 5.0 V, I_D = 45 A			120		S
CHARGES, CAPACITANCES AND GATE RESISTANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			2900		pF
Output Capacitance	C_{oss}				1300		
Reverse Transfer Capacitance	C_{rss}				28		
Total Gate Charge	$Q_{G(TOT)}$	V_{DS} = 48 V, I_D = 45 A	V_{GS} = 4.5 V		17		nC
			V_{GS} = 10 V		39		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 45 A			4.8		nC
Gate−to−Source Charge	Q_{GS}				8.8		
Gate−to−Drain Charge	Q_{GD}				3.5		
Plateau Voltage	V_{GP}				3.2		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 45 A, R_G = 2.5 Ω			21		ns
Rise Time	t_r				91		
Turn−Off Delay Time	$t_{d(off)}$				47		
Fall Time	t_f				68		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 45 A	T_J = 25°C		0.9	1.2	V
			T_J = 125°C		0.8		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 45 A			47		ns
Charge Time	ta				23		
Discharge Time	tb				24		
Reverse Recovery Charge	Q_{RR}				30		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
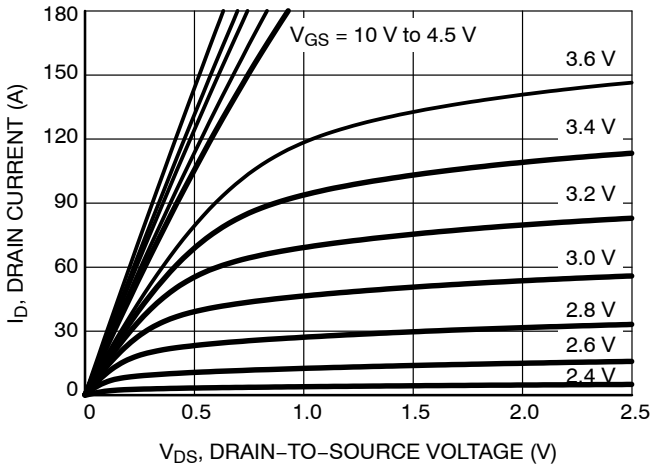
NVD5C648NL

TYPICAL CHARACTERISTICS

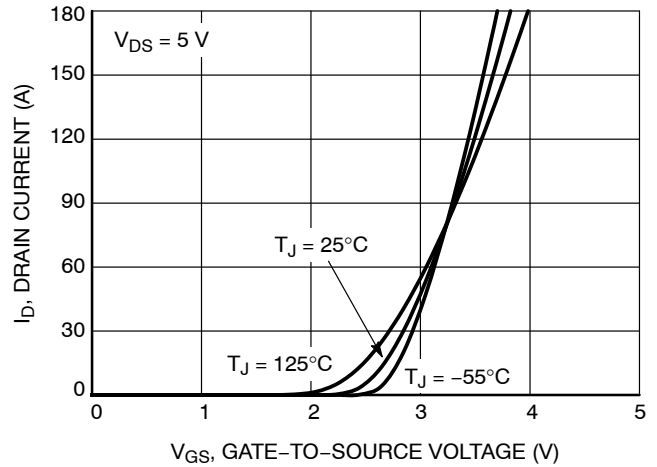Figure 1. On−Region Characteristics

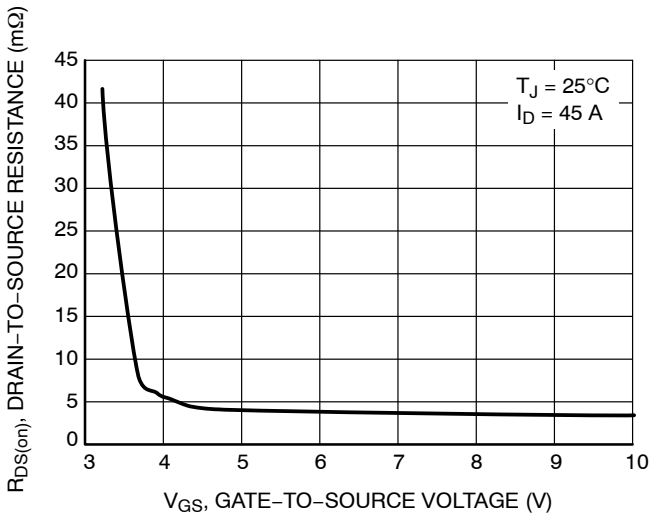Figure 2. Transfer Characteristics

Figure 3. On−Resistance vs. Gate−to−Source Voltage
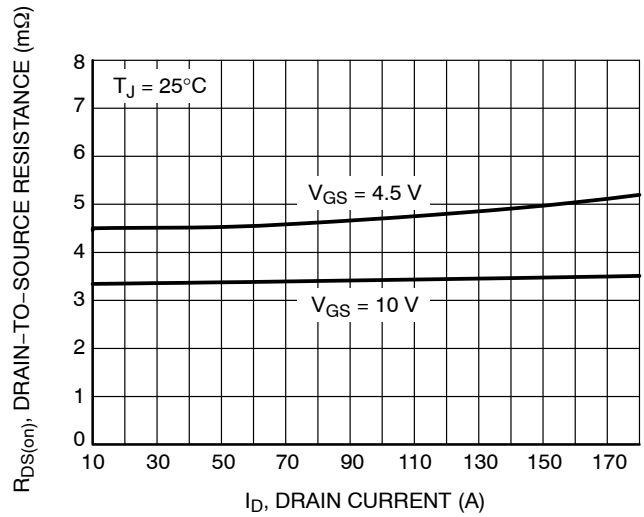

Figure 4. On−Resistance vs. Drain Current and Gate Voltage
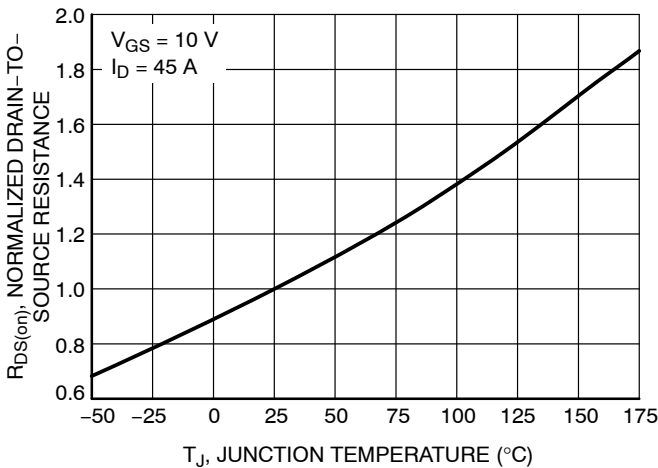

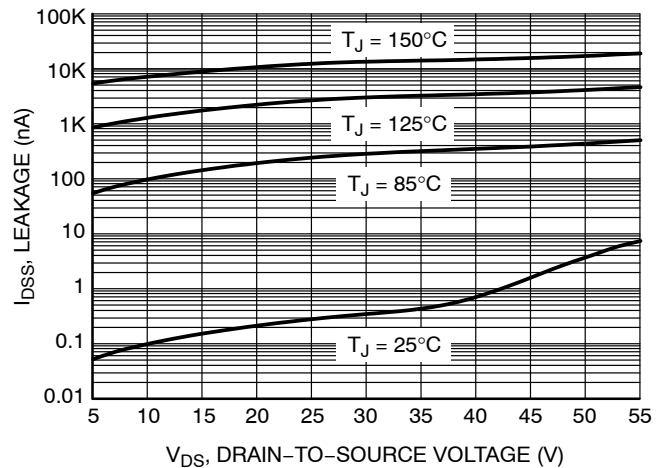Figure 5. On−Resistance Variation with Temperature

Figure 6. Drain−to−Source Leakage Current vs. Voltage
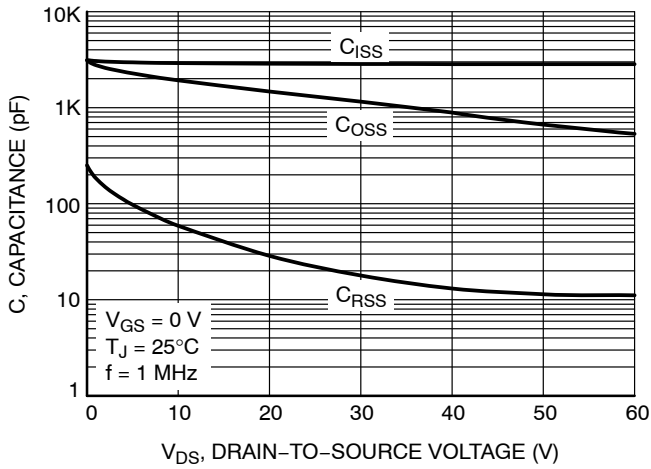
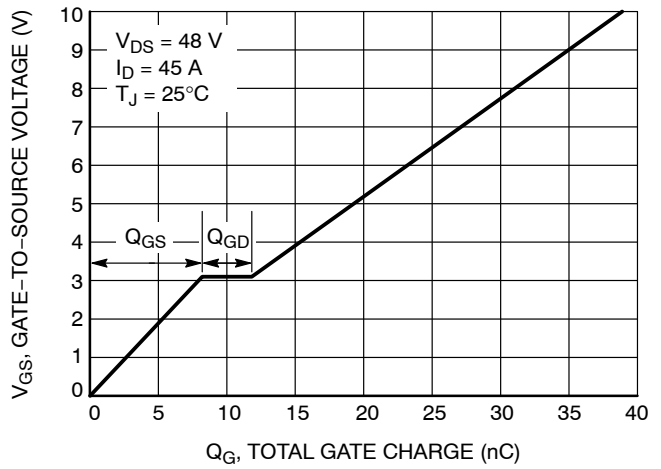## TYPICAL CHARACTERISTICS

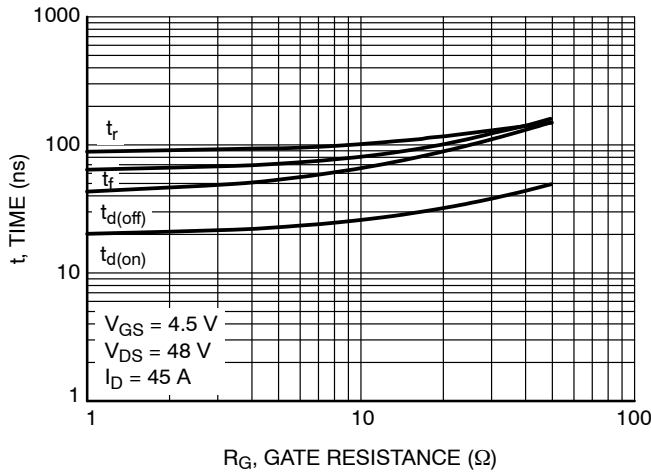Figure 7. Capacitance Variation

Figure 8. Gate−to−Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
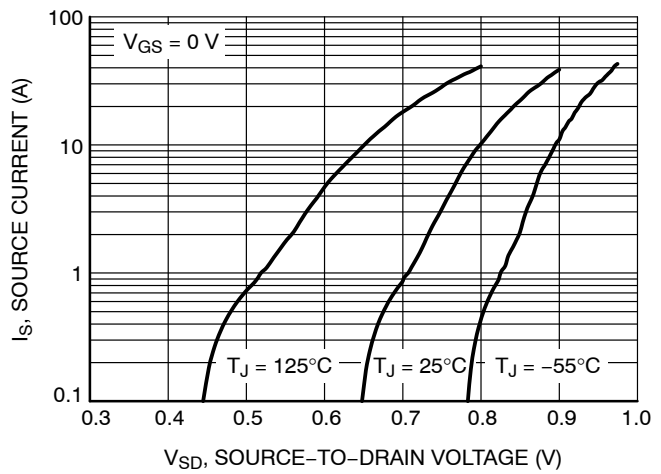
Figure 10. Diode Forward Voltage vs. Current
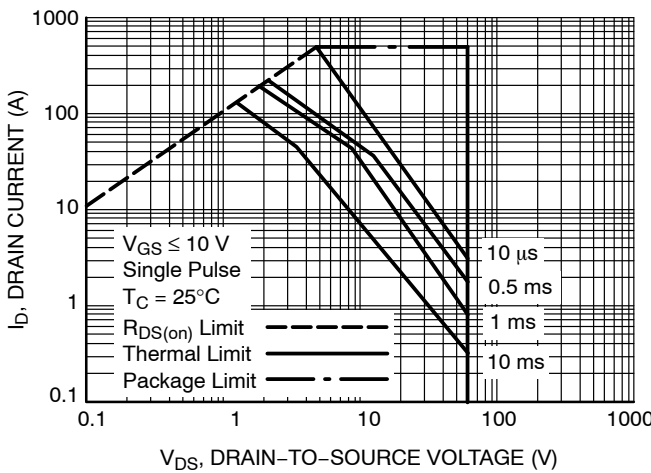
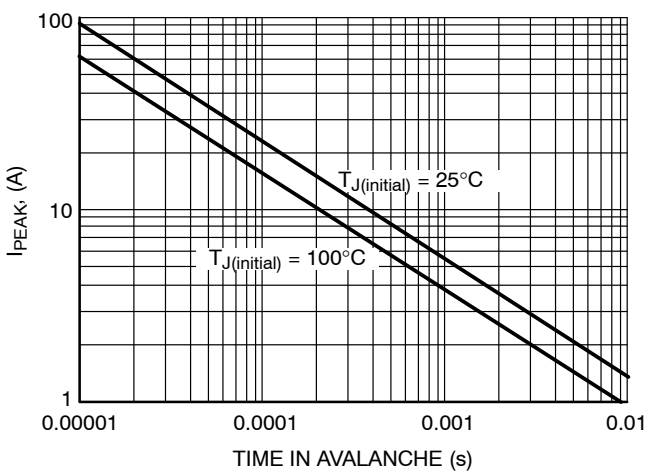Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Drain Current vs. Time in Avalanche
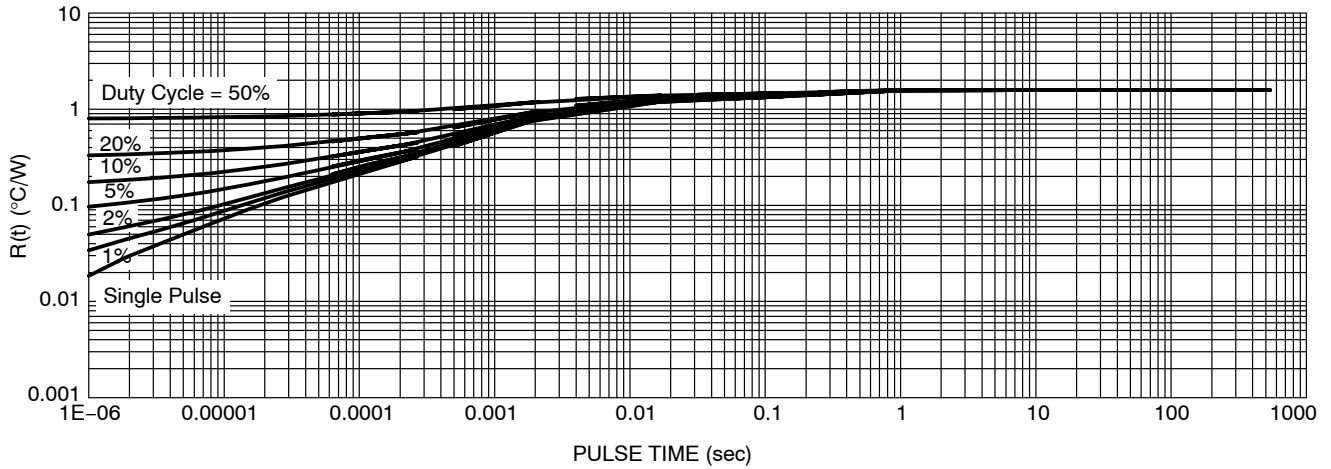
NVD5C648NL

TYPICAL CHARACTERISTICS
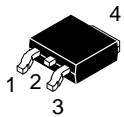

Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping[†]
NVD5C648NLT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

SCALE 1:1

TOP VIEW $\oplus$ | 0.005 (0.13) Ⓜ | C

SIDE VIEW

DETAIL A

BOTTOM VIEW

BOTTOM VIEW
ALTERNATE
CONSTRUCTIONS

DETAIL A
ROTATED 90° CW
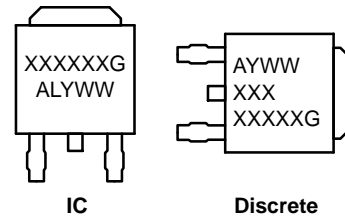
GAUGE PLANE
SEATING PLANE
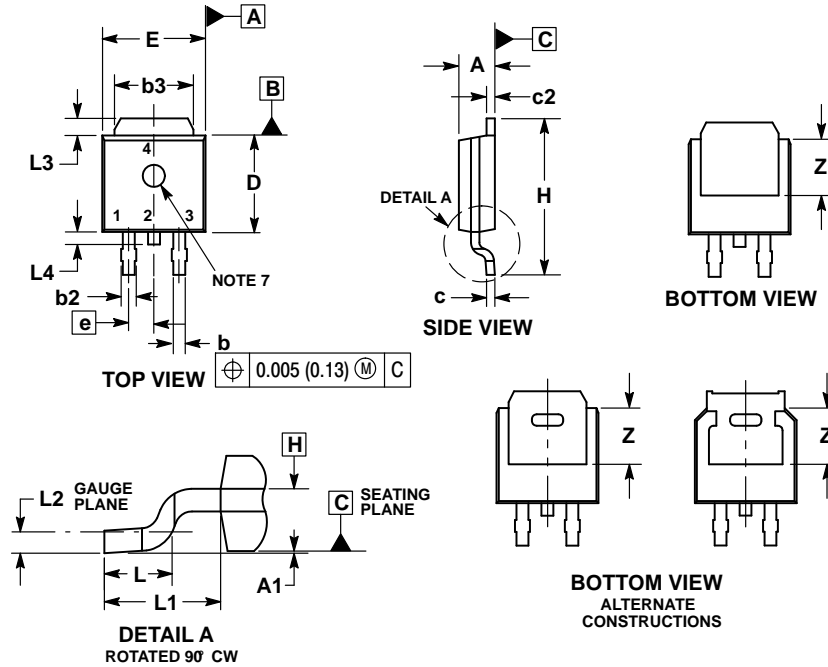
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

XXXXXXG
ALYWW

IC

AYWW
XXX
XXXXXG

Discrete
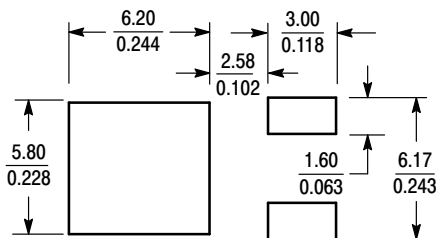
XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*

6.20 / 0.244
3.00 / 0.118
2.58 / 0.102
5.80 / 0.228
1.60 / 0.063
6.17 / 0.243

SCALE 3:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON10527D	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:	REF TO JEDEC TO−252	
DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOUNT	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

PUBLICATION ORDERING INFORMATION

◊

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#):
  [NVD5C648NLT4G](#)